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(convert or conversion or translate or translation) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) and (hierarchy or hierarchical)) and (store or storage or database)  ((((((VMDL or MDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect\$3 or locat\$3 or find\$3)))  72 (((((((VMDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3))) and DERWENT;			(ASIC or FPGA) and ((hardware same		
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property))) and (hierarchy or hierarchical)) and (store or storage or database)  ((((((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect\$3 or locat\$3 or find\$3)))  (((((((((WHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)))) and DERWENT;			adj module) or (design adj element) or		
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simulat\$3) or (logic same simulat\$3)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect\$3 or locat\$3 or find\$3)))  [((((((((VHDL or HDL or (schematic adj c)) uSPAT; and (ASIC or FPGA) and ((hardware same simulat\$3))) and DERWENT;		, 2			2003/05/02 21:19
<pre>(convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect\$3 or locat\$3 or find\$3)))  72 ((((((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3) or (logic same simulat\$3))) and DERWENT;</pre>				-	
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72 ((((((((VHDL or HDL or (schematic adj c)) USPAT; and (ASIC or FPGA) and ((hardware same JPO; simulat\$3)) or (logic same simulat\$3)) and DERWENT;			(debug or debugging or (error same (detect\$3		
and (ASIC or FPGA) and ((hardware same JPO; simulat\$3) or (logic same simulat\$3)) and DERWENT;		70			2002/05/25
simulat\$3) or (logic same simulat\$3)) ) and DERWENT;	-	/2	· · · · · · · · · · · · · · · · · · ·	,	2003/05/02 21:29
			(convert or conversion or translate or	IBM_TDB	
translation)) and (documentation or				1 TBM_1 DB	
description or recommendation)) and ((design					
adj module) or (design adj element) or					
(core) or (IP) or (intellectual adj					
property))) and (hierarchy or hierarchical))	] [				
and (store or storage or database)) and			and (store or storage or database)) and		
(debug or debugging or (error same (detect\$3					
or locat\$3 or find\$3))) and (link\$3 or			or locat\$3 or find\$3)))) and (link\$3 or		
I	L		connect\$3 or associat\$3)		

-	145	<pre>(((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3) or (logic same simulat\$3)) ) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)))</pre>	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:31
	0	(((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)) or (logic same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link\$3 or connect\$3 or associat\$3) same (simulation with (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:34
	2	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)) or (logic same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link\$3 or connect\$3 or associat\$3) same (simulat\$3 same (result or data or info or information	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:35
	6	or vector)))  ((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)) or (logic same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link\$3 or connect\$3 or associat\$3) same ((simulat\$3 or test\$3) same (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:38
-		<pre>((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3) or (logic same simulat\$3)) ) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link\$3 or connect\$3 or associat\$3)) (VHDL) and (high adj level) and (physical)</pre>	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:08 2003/05/05 10:10
		adj implementation)	JPO; DERWENT; IBM_TDB	

-	0	(VHDL) and ((high adj level) same (physical	USPAT;	2003/05/05 10:11
		adj implementation)) same ((data adj base)	JPO;	1
		or (database))	DERWENT;	
			IBM TDB	
-	77	((VHDL) and (high adj level) and (physical	USPAT;	2003/05/05 10:11
1		adj implementation)) and database	JPO;	
		, .	DERWENT;	
			IBM TDB	
-	2	(((VHDL) and (high adj level) and (physical	USPAT;	2003/05/05 10:11
		adj implementation)) and database) and	JPO;	
		testbench	DERWENT;	]
			IBM TDB	
-	3	object same oriented same VHDL same database	USPAT;	2003/05/06 13:43
			EPO; JPO;	
			IBM TDB	
-	223	(rostocher).in. OR (dangelo).in.	USPAT;	2003/05/06 13:45
		_	EPO; JPO;	
			IBM TDB	
-	8	(hierarch\$4 or generation\$2 or tree or	USPAT;	2003/05/06 13:45
		child\$3) same VHDL same database	EPO; JPO;	
			IBM_TDB	1